Atacama
Large
Millimeter
Array

Interface Control Document

Between 64-Antenna Correlator
And Correlator Computing System

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1 Description

1.1 Purpose

This ICD covers the cabling / electrical interface requirements between the correlator and the CCC, CDP and DMC computers. The software / control function interface is included by reference to the detailed CAN protocol plans, discussed in the next section.

1.2 Scope

The ALMA correlator processes signals from a total of 64 antennas, in four separate correlator quadrants, one quadrant for each of the four baseband pairs. All four quadrants are controlled and monitored by a single Correlator Control Computer (CCC). Each individual quadrant produces data to be processed by a cluster of four Correlator Data Processing (CDP) computers (16 CDP computers total for the four correlator quadrants). There is one additional Master CDP computer.

There is one backup CCC and one backup Master CDP computer. These computers will normally be in a powered down state but physically connected to all necessary interfaces so they may quickly substitute for the primary computers in response to remote commands.

There are two computers identified as DMC's which provide the eight CAN bus interfaces for the DRX modules (Data Transmission System Receiver module) that are located in the correlator. The DRX modules are installed in the correlator system racks but are the responsibility of the Backend IPT.

The Correlator System Racks consist of eight racks in each of four quadrants. In each correlator quadrant the eight system racks consist of four racks identified as Station Racks and four racks identified as Correlator Racks.

There are four Data Port Interface (DPI) modules in each quadrant, one per CDP computer. The DPI modules are the responsibility of the correlator IPT but are physically installed in the same rack as the CDP computers. The DPI modules provide the high speed data output paths for correlator results.

Correlator system CAN bus nodes are tabulated in section 9. DRX (Backend IPT) CAN node assignments are identified in [RD 11].

2 Related Documents and Drawings

2.1 CAN Protocol Definition Documents

The detailed definitions of the communication protocols between CCC and each control card in the correlator are still under development. They are evolving along with the control software for CCC and the embedded software in the correlator control cards. These documents are formally maintained in the CVS system along with the embedded software and firmware (FPGA designs). PDF copies of the protocols are provided in ALMA edm for reference. The CVS revisions, as of 2007-07-09, are included in the following table.

Reference Number	Document Number	Title	CVS Rev
[RD 01]	CORL-60.02.03.00-001-B-PLA	CAN Protocol Plan: between CCC and LTA	1.14
[RD 02]	CORL-60.01.05.00-001-B-PLA	CAN Protocol Plan: between CCC and SCC	1.10
[RD 03]	CORL-60.02.05.00-001-B-PLA	CAN Protocol Plan: between CCC and QCC	1.2
[RD 04]	CORL-60.02.04.00-001-A-PLA	CAN Protocol Plan: between CCC and FA	1.1
[RD 05]	CORL-60.03.02.00-001-A-PLA	CAN Protocol Plan: between CCC and DPI	1.1

2.2 Other Documentation

[RD 06] User Manual for the PCI64-HPDI32 Card, General Standards Corporation (www.generalstandards.com)

[RD 07] User Manual for the Infineon C167 Microprocessor (www.infineon.com)

[RD 08] User Manual for the TPMC901 CAN Bus PMC Module.

[RD 09] ALMA Monitor and Control Bus Interface Specification, ALMA-70.35.10.03-001-B-SPE

[RD 10] Control and Communication Cable Plan, CORL-60.05.00.00-003-A-PLA (Correlator IPT EDM document number 147)

[RD 11] ALMA-53.09.00.00-70.35.30.00-B-ICD,
Interface Control Document Between
Back-End/DTS Receiver Module And Computing/Control Software

[RD 12] ALMA-20.01.02.00-60.00.00.00-A-ICD,
ICD between AOS Technical Building and Baseline Correlator

2.3 Abbreviations and Acronyms

CAN	Controller Area Network
CCC	Correlator Control Computer
CDP	Correlator Data Processing Computer
CVS	Concurrent Versions System
DMC	DRX Monitor and Control Computer
DPI	Data Port Interface Module
DRX	DTS Receiver Module
DTS	Data Transmission System
IDC	Insulation Displacement Connector
LTA	Long Term Accumulator Card
LVDS	Low Voltage Differential Signaling
SCC	Station Control Card
QCC	Quadrant Control Card
TE	Time Event

3 Interface Signal Categories, Types and Cable Lengths

There are four categories of signal types between the correlator and computer systems:

Signal Type	Description
CAN Bus	CAN buses between computer and correlator and between DRX modules and computer.
TE	48 msec time event from correlator to computer.
Correlator Output Data	High data rate parallel output interfaces from correlator to computer.
RESET	Reset signal from computer to correlator.

Table 1, Correlator ←→ Computer Signal Categories

The signal interfaces consist of four different industry standard electronic signal levels:

CAN bus logic levels
RS-232 single ended levels
RS-485 differential levels
LVDS (Low Voltage Differential Signaling) levels

3.1 Phasing of TE signals to computers w.r.t. TE from Backend

The TE signals are generated by the QCC as a function of the TE signal provided by the Backend IPT to the Correlator.

The TE signals to the CCC, CDP and DMC computers will all be phased identically, within 1 usec of the TE from the Backend.

3.2 Signal Cable Lengths

The lengths of cables are not defined in this ICD. The correlator IPT will be responsible for identifying the lengths needed in all cases when fabricating the cables.

4 Summary of Correlator IPT Responsibilities

The following table lists all cables and other items to be provided by the correlator IPT, as defined in this ICD. In the text, correlator IPT responsibilities are *shown in blue* for emphasis.

Item #	QTY	Description	Section
1	2	TE cables, Correlator to CCC computers	6.1
2	1	CAN Flat cable : CCC → Backup-CCC → adapter	6.2.1
3	1	Breakout Adaptor from item 2 to item 4	6.2.1
4	5	Individual CAN cables, one per correlator CAN bus	6.2.2
5	8	DMC to DRX CAN cables, one per DRX CAN bus	7.1
6	2	TE cable, correlator to DMC	7.2
8	2	TE cables, Correlator to Master CDP computers	8.2
9	4	RESET cables, CDP computers to Correlator	8.3

5 Summary of Computer IPT Responsibilities

The next table lists all items to be provided by the computer IPT, as well as other responsibilities of the computer IPT. In the text, computer IPT responsibilities are *shown in green* for emphasis.

Item #	Quantity	Description	Section
1	na	Insure TPMC901 internal terminations properly selected	6.2
2	8	CAN bus terminators for DMC	7.1
3	16	DPI to CDP data interface cable	8.1
4	na	Provide rack space in CDP racks for four DPI, *mounted at adjacent 2U locations*	8.1

6 Corr ←→ CCC

The Backup-CCC computer is configured as a "fully connected spare", so the physical interfaces between the correlator and both CCC computers are always connected and available for use. There are two categories of signals: CAN Bus and TE.

6.1 CCC Time Event (TE) Interface (2 TE cables)

The correlator sources the 48 msec Time Event signals to the CCC and Backup-CCC computers. The CCC computers use a standard RS-232 serial port (e.g. "COM1") as the input port for the TE signal. The QCC generates the TE signal. The TE from the QCC drives a TE distributor, physically located in a Data Port Interface (DPI) enclosure. The TE distributor provides the two RS-232 outputs required by the two CCC computers.

The correlator IPT will provide the set of two cables for this interface, one for CCC and one for Backup-CCC. Category 5 LAN type cable, with **D-Type 9 pin female** connectors on the CCC end, will be provided with the following pin out assignments at the CCC and Backup-CCC COM port connector interface points:

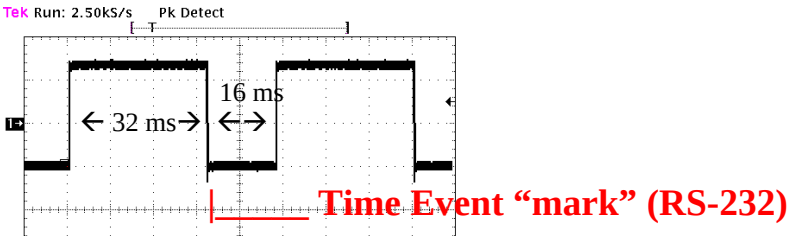
CCC end of cable	←Cable *IS* straight through → CTS and GND *are* a twisted pair	Corr end of cable

DB-9F Pin	**Serial Port Signal Name**	**DB-9F Pin**	**Correlator Signal Name**
1			
2			
3			
4			
5	Ground	**5**	GND
6			
7			
8	**CTS**	**8**	***TE (RS-232)***
9			

Table 2, CCC TE Signal Connector Pin Assignments

The duty cycle of the TE signal is 16 msec / 32 msec (48 msec period). As generated by the QCC, the TE signal is high for the 16 msec portion of the period. **The time event mark is defined as the leading edge of the 16 msec wide pulse.**

The standard RS-232 serial port signals are logically inverted on the interface with respect to the driving signal, so the leading edge that marks the precise time event is seen as a falling edge when viewed with a scope on the interface. The serial interface in the CCC computer logically inverts this signal one more time so that the time event signal is found to be logically high for 16 msec and low for 32 msec when detected by the CCC interrupt handler. The scope photo below shows the CTS signal at the RS-232 interface, where the leading edge of the 16 msec pulse is a falling edge:



6.2 CAN Bus Interface

The CCC and Backup-CCC computers each have a TPMC901 six port CAN bus controller interface module. In order to provide the "fully connected spare" capability, both computers are always connected together on each of the six CAN buses. The two CCC computers are physically located at one end of the bus. It is necessary that a standard line to line CAN bus termination be provided at each end of the bus. The TPMC901 module has internal terminations that are jumper selectable. In order to properly terminate the bus, it is necessary that the internal terminations be selected in the TPMC901 module that is physically at the end of the bus and not selected in the second TMPC901 module. *The computer IPT will be responsible for insuring that the internal terminations in the TPMC901 modules are configured correctly.*

6.2.1 Flat cable Assembly and Breakout Adaptor (1 flat cable, 1 breakout adaptor)

The correlator IPT will provide the required cable assembly to connect the two CCC computers together and the adaptor to breakout the six individual CAN buses (5 assigned to the correlator, 1 spare).

The cable assembly to connect the two CCC computers together will consist of one span of 13 pair twisted flat cable (12.5 pairs used), with IDC connectors installed at three locations on the cable, plus one DB-25 to DB-9 adaptor, as shown in the next figure. Pin assignments for the TPMC901 module, and the wiring assignments for the breakout adaptor, are provided for reference in section 12 .

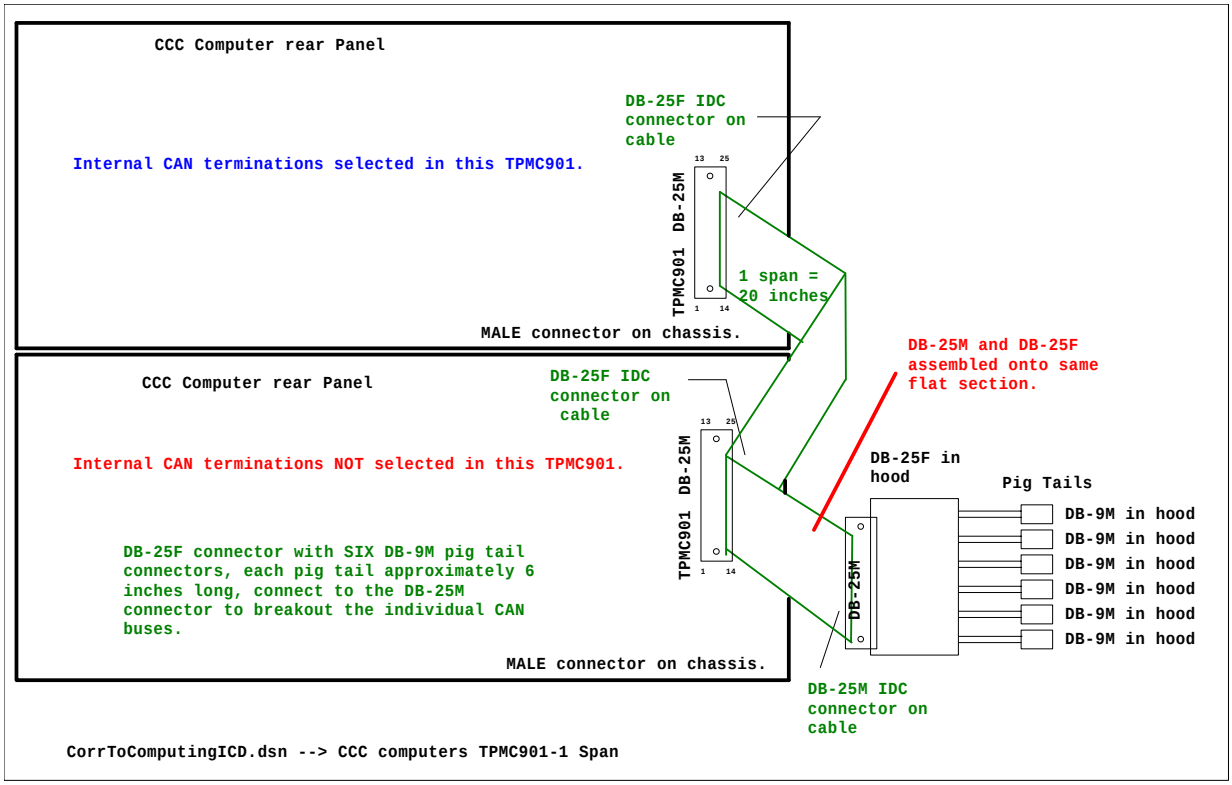

CCC Computer rear Panel
Internal CAN terminations selected in this TPMC901.
DB-25F IDC connector on cable
TPMC901 DB-25M
1 span = 20 inches
MALE connector on chassis.
CCC Computer rear Panel
Internal CAN terminations NOT selected in this TPMC901.
DB-25F IDC connector on cable
DB-25F connector with SIX DB-9M pig tail connectors, each pig tail approximately 6 inches long, connect to the DB-25M connector to breakout the individual CAN buses.
MALE connector on chassis.
DB-25M and DB-25F assembled onto same flat section.
DB-25F in hood
Pig Tails
DB-9M in hood
DB-9M in hood
DB-9M in hood
DB-9M in hood
DB-9M in hood
DB-9M in hood
DB-25M IDC connector on cable
CorrToComputingICD.dsn --> CCC computers TPMC901-1 Span

Figure 6.1, CCC CAN Bus Interface Flat Cable / Breakout Adaptor Assembly

6.2.2 Individual CAN Cables (5 CAN cables)

The correlator IPT will provide the five cables that connect to the pigtails at the breakout adaptor to drive the correlator CAN buses. Category 5 LAN type cable will be used for the cables. The cables are wired straight through as defined in the following table. The connector type on both ends of the cable is DB-9 Female.

CCC end of cable	←Cable *IS* straight through → CAN-L and CAN-H *are* assigned to a single twisted pair	Corr end of cable

DB-9F Pin	Signal Name	DB-9F Pin
1		1
2	CAN-L	**2**
3	GND	**3**
4		4
5		5
6		6
7	CAN-H	**7**
8		8
9		9

6.2.3 CAN Bus Length and Configuration Options

Typically, a length of 40 meters maximum is specified for operation at the 1 Mbit/sec rate in use, as seen in the calculations from the C167 User Manual, [RD 07], shown below. The bus line delay used in this calculation is based on a 40 meter total bus length.

40 m length →

Bit Timing Example for High Baudrate

This example makes the following assumptions:

- XCLK frequency = 20 MHz
- BRP = 00, CPS = 0
- Baudrate = 1 Mbit/sec

t_q	100 ns	$= 2 \times t_{XCLK}$
bus driver delay	50 ns	
receiver circuit delay	30 ns	
bus line (40 m) delay	220 ns	
t_{Prop}	600 ns	$= 6 \times t_q$
t_{SJW}	100 ns	$= 1 \times t_q$
t_{TSeg1}	700 ns	$= t_{Prop} + t_{SJW}$
t_{TSeg2}	200 ns	= *Information Processing Time*
t_{Sync}	100 ns	$= 1 \times t_q$
t_{Bit}	1000 ns	$= t_{Sync} + t_{TSeg1} + t_{TSeg2}$
tolerance for t_{XCLK}	0.39%	$= \frac{\min(PB1, PB2)}{2 \times (13 \times \text{bit time} - PB2)}$
		$= \frac{0{,}1\mu s}{2 \times (13 \times 1\mu s - 0{,}2\mu s)}$

See section 14 for discussion of the CAN bus configuration options that have been considered for use in the correlator. In brief, there is the five bus option presented here, a six bus option, and a nine bus option. *So far, results in the first quadrant demonstrate that error free operation is possible with the selected five bus option. But the maximum bus length with this option approaches the 40 m limit*. The six bus and nine bus options are still considered as possible fall backs if operation in the final four quadrant configuration does not produce error free operation in all four quadrants.

6.2.4 Correlator CAN node RESET

The global RESET signal for all correlator CAN nodes (excluding the QCC nodes) is not directly interfaced to the CCC computer. This signal is internally driven by the Quadrant Control Card (QCC) in response to a CAN command from CCC to the QCC. A separate RESET signal from CCC to QCC is covered in section 8.3.

7 Corr ←→ DMC

There are three categories of signals defined for this interface, the CAN bus for the DRX modules, the RESET signal for the DRX CAN buses, and a TE signal provided as an input to the DMC. See section 15 for a sketch of the bus routing inside the correlator.

7.1 DMC to DRX CAN Bus and RESET (6 CAN cables, 6 Terminators)

The I/O panel on the DMC combines the CAN and RESET signals into individual DB-9 panel mount connectors. The I/O panel provides pairs of DM-9 male and female connectors, one pair for each CAN bus. The CAN bus signals are the industry standard CAN_H / CAN_L signals. The RESET signals are industry standard RS-485 differential RSTB / RSTA signal pairs.

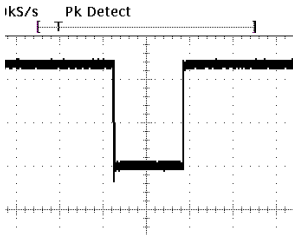
For each CAN bus, a terminator installs on the female panel mounted connector and the CAN cable (which carries the CAN bus and the RESET signals) plugs onto the male panel mounted connector. Thus the cable has a female DB-9 on the DMC end. Tensolite NF24Q100 Ethernet type 100BASE-T cable will be used.

The correlator IPT will provide the six DB-9 CAN cables from the DMC I/O panel to the Station racks.

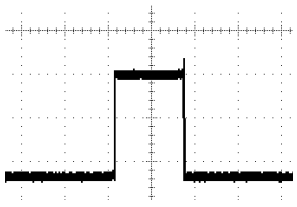
The computer IPT will provide the six terminator assemblies on the I/O panel.

The RS-485 signals are shown below to identify the asserted state:

RSTA



RSTB



|_____ RESET asserted (RS-485) width per [RD 09]

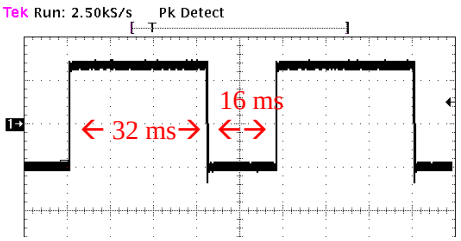
[RD 09] section 2.2.6 specifies that the reset state is asserted when RSTB is high and RSTA is low. The reset duration is determined by the DMC computer per [RD 09]. See section 13.2 for details of the pin assignments at the interface point on the DMC I/O panel, as per [RD 09] Figure 1. In the station backplanes, the RSTA and RSTB signals from the DMC will drive the corresponding DRX inputs.

7.2 DMC TE Signal Interface (two TE cables)

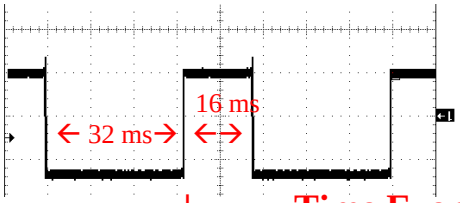
The TE signal to the DMC is connected to a separate Molex connector on the DMC I/O panel. The TE signal is an industry standard RS-485 differential TE-B / TE-A signal pair.

The correlator IPT will provide the cable that connects to the panel mount Molex connector.

TE-A



TE-B



Time Event "mark" (RS-485)

The duty cycle of the TE signal provided by the correlator is 16 msec / 32 msec (48 msec period). [RD 09] section 2.2.7 specifies that the timing event is marked by the rising edge of TE-B (which corresponds to the falling edge of TE-A).

See section 13.1 for details of the pin assignments on this interface, as per [RD 09].

8 Corr ←→ CDP

There are three types of interface signals to/from the CDP computers. One is the high speed correlator output data bus. One is the system TE, and the third is the RESET signal.

8.1 High Speed Data Interface (16 data cables)

For each correlator quadrant there are four CDP computers interfaced to four correlator Data Port Interface (DPI) rack mount modules. These modules are each 2U high. The four DPI modules are mounted in the same rack as the four CDP computers. *The four DPI modules are installed in a single stack in the rack at four adjacent 2U locations.* The adjacent location requirement is necessary to minimize the total length of the correlator CAN bus.
The CDP end of the data interface uses a commercial High-Speed Parallel Digital Interface that installs in the PCI bus of the CDP computer. This is a PCI64-HPDI32A PCI card from General Standards Corporation. The interface signal levels are LVDS.

The physical cables between the correlator and the CDP computers are from the same commercial source as the PCI cards. The cable is part number CABLE6 SH-PCI64-HPDI32AL-LVDS, a six foot long cable, using Robinson Nugent connectors on each end, part number P50E-080-S-TG (50 mil twisted pair cable). This cable mates with the 80 pin CDP interface connector and with the DPI board mount connectors (Robinson Nugent part number P50E-080-P1-SR1-TG). *The cables are provided by the computer IPT.*

See the referenced users manual for the PCI64-HPDI32A interface card [RD 06] for the specific pinout of the 80 pin connector. The cable provides a 1 to 1 straight through connection.

The TE signal from the correlator to the CDP computers is provided over this same interface, so there is not a separate TE input to these computers.

8.2 Correlator to Master CDP TE Interface (2 TE cables)

The Master CDP and Backup-Master CDP computers do not have the high speed data interface, so the TE signal is provided separately. The interface is identical to the CCC Time Event interface covered in section 6.1.

The correlator IPT will provide the two cables to connect the TE signal to the Master CDP and Backup-Master CDP computers.

8.3 CDP to Correlator RESET Interface (4 RESET cables)

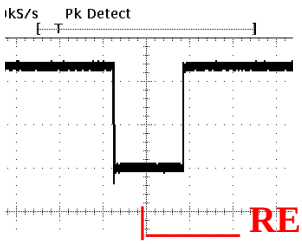
The QCC in each quadrant has a RS-485 differential input signal that may be used to force a hard reset of the microprocessor. In each quadrant, the RESET signal will be driven from the RS-232 COM port on one of the four CDP computers that handle the high speed output from the quadrant. The RTS output from the CDP COM port will be used. The RS-232 signal will be converted to RS-485 in one of the TE distributors, internal to the correlator.

The correlator IPT will provide the set of four cables for this interface. Category 5 LAN type cable, with **D-Type 9 pin female** connectors on the both ends, will be provided with the following pin out assignments:

CCC end of cable	←Cable *IS* straight through → RTS and GND *are* a single twisted pair	Corr end of cable

DB-9F Pin	**Serial Port Signal Name**	**DB-9F Pin**	**Correlator Signal Name**
1			
2			
3			
4			
5	Ground	**5**	GND
6			
7	**RTS**	**7**	***RESET (RS-232)***
8			
9			

The standard RS-232 serial port signals are logically inverted on the interface with respect to the driving signal. Thus when viewed on a scope connected to the RS-232 RTS signal, when RTS is asserted, the RS-232 signal will be at the negative level as shown in the following figure:



RESET asserted (RS-232)
width > 1 msec

9 CAN Node Assignments

The CCC controls and monitors the correlator using one CAN bus per quadrant plus one CAN bus for the four Quadrant Control Cards. Each CAN node is an internal peripheral of an Infineon C167 microprocessor.

The QCC cards are assigned to nodes 20-23 for historical reasons.

The Final Adder card nodes are assigned so that they identify which quadrant the four "main" CAN buses are connected to.

9.1 Main CAN bus in each quadrant

Nodes	Quad 1	Quad 2	Quad 3	Quad 4
0-15	LTA	LTA	LTA	LTA
16-31	SCC	SCC	SCC	SCC
32-34	Not assigned; 32-33 presently used for DTSsims in first quadrant			
35-36	FA			
37-38		FA		
39-40			FA	
41-42				FA
43-46	DPI	DPI	DPI	DPI
47	Not available (this is the "recovery" address for corrupted applications)			
48-59	Not assigned			
60-63	Reserved for various test fixture special cases			

9.2 QCC CAN bus (single bus to all four quadrants)

Nodes	Quad 1	Quad 2	Quad 3	Quad 4
20	QCC			
21		QCC		
22			QCC	
23				QCC

10 Software/Control Function Interface

The control function protocols are defined in the referenced CAN Protocol Plan documents.

11 Mechanical, Electrical Power, Thermal and Safety Interfaces

The physical interfaces consist of signal cables and the DPI modules. The DPI module is logically an internal component of the correlator, but physically resides in computer system racks, and thus is included in this section.

11.1 Mechanical Interface

The only item with a mechanical interface is the DPI module. The DPI modules are standard 19 inch rack mount enclosures, 2U high. This enclosure is manufactured by Hammond, part number RMCV1903BK1. There is one DPI module for each CDP computer, four modules in each CDP rack. Each enclosure is mounted in the rack using chassis slides. It is a requirement that the four DPI enclosures in a single CDP rack be mounted at adjacent 2U positions in the rack.

11.2 Electrical Power Interface

The DPI module contains a built-in AC-DC power supply, operating from an AC input of 85 - 265 VAC, 47 - 440 Hz. The power supply is an Astrodyne Model AS-40-5. The DPI modules will use standard AC power cords and will be powered from the same UPS system that powers the computers. The total AC power requirement for the four DPI modules in one rack is less than 40 watts.

11.3 Thermal Interface

The only item requiring cooling is the DPI. The DPI module is cooled by an internal fan, operated from the internal 5V power supply, using ambient air.

11.4 Safety Interface

In all respects, the cables and DPI modules are considered to be integral parts of the correlator system, and as such are subject to the same safety requirements as specified in sections 5.2 and 5.3 of [RD 12], ALMA-20.01.02.00-60.00.00.00-A-ICD. The signal types, defined in section 3, are all low voltage type signals.

12 TPMC901 DB-25M Connector Pin Assignments

Pin assignments for the six CAN channels at the TPMC901 DB-25M connector are shown in the table to the right and the assignments to the six DB-9F pigtail connectors are shown in the tables below.

7 Pin Assignment

7.1 Front Panel I/O

Pin	TPMC901-10
01	GND
14	CAN Low Channel 0
02	CAN High Channel 0
15	GND
03	GND
16	CAN Low Channel 1
04	CAN High Channel 1
17	GND
05	GND
18	CAN Low Channel 2
06	CAN High Channel 2
19	GND
07	GND
20	CAN Low Channel 3
08	CAN High Channel 3
21	GND
09	GND
22	CAN Low Channel 4
10	CAN High Channel 4
23	GND
11	GND
24	CAN Low Channel 5
12	CAN High Channel 5
25	GND
13	NC

Figure 7-1

DB-9F Chan 0	DB-25M Chan 0	Signal	DB-25M Chan 1	DB-9F Chan 1
1				1
2	14	CAN Low	16	2
3	1,15	Signal Gnd	3,17	3
4				4
5				5
6				6
7	2	CAN High	4	7
8				8
9				9

DB-9F Chan 2	DB-25M Chan 2	Signal	DB-25M Chan 3	DB-9F Chan 3
1				1
2	18	CAN Low	20	2
3	5,19	Signal Gnd	7,21	3
4				4
5				5
6				6
7	6	CAN High	8	7
8				8
9				9

DB-9F Chan 4	DB-25M Chan 4	Signal	DB-25M Chan 5	DB-9F Chan 5
1				1
2	22	CAN Low	24	2
3	9,23	Signal Gnd	11,25	3
4				4
5				5
6				6
7	10	CAN High	12	7
8				8
9				9

The two GND pins for each channel from the TPMC901 DB-25M are both wired to a single GND pin in the corresponding DB-9F connector. Twisted pairs are used for CAN-L / CAN-H.

13 DMC I/O Panels

The I/O panel on the DMC provides six pairs of DB-9 male/female connectors for the CAN Bus / RESET signals, and a single 3 pin Molex connector for the TE signal.

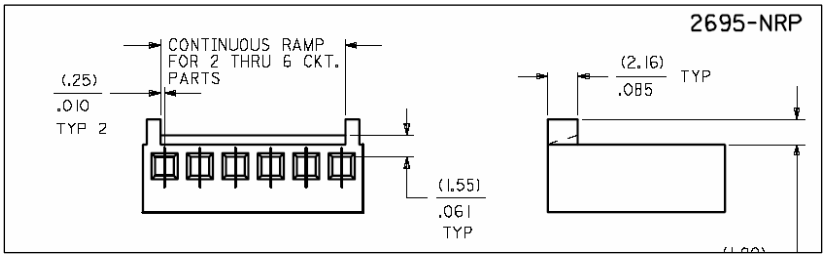
13.1 DMC TE Connector Interface

The mating connector housing for the Molex connector, provided on the TE cable from the correlator, is Molex part number 22-01-3037. Connector details are provided in the following figures which were extracted from the Molex data sheet.

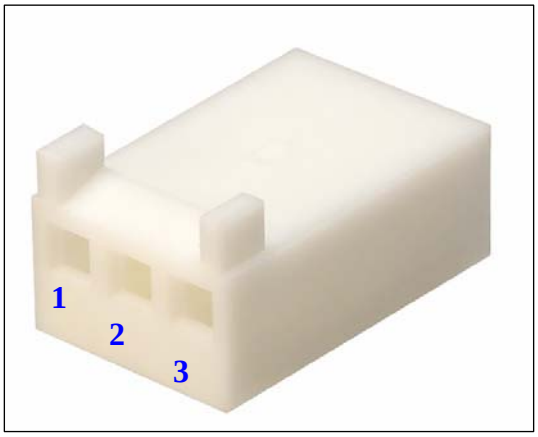
PART NO.	ENG NO.
N/A	2695-1RP
22-01-3027	2695-2RP
→ 22-01-3037	2695-3RP

The part number is cross referenced above to the 2695-3RP engineering number that in turn maps to the following drawing:

where N=3
R = “ramp”
P = Polarizing ribs



and here is a photo with pin numbers added:



Digikey PN for housing is WM-2001 (Molex #22-01-3037);

for contacts it is WM1114 (Molex #08-50-0114)

The cable wiring is defined in the following table:

DMC end of cable	← Cable is *NOT* straight through → TE-B / TE-A are assigned to a single differential pair CAT5 type cable will be used	**Corr end of cable**

Molex Pin#	**Signal**	**Description**	**DB-9M Pin#**
2	TE-B	RS-485 differential “true” signal	1
			2
			3
			4
3	GND	GND	5
1	TE-A	RS-485 differential “bar” signal	6
			7
			8
			9

The I/O panel Molex connector is the interface point. The cable is provided by the correlator group. The source of the TE signal is from a DB-9 type connector on an internal TE distributor module that is mounted in a DPI enclosure.

[RD 09] section 2.2.7 specifies that the timing event is marked by the rising edge of TE-B (which corresponds to the falling edge of TE-A).

13.2 DMC CAN Connector Interface

As per [RD 09], Figure 1 and Table 1, the following pin assignments define the signals on each pin of the DB-9 female connector on the end of the cable provided by the correlator IPT. NOTE : *A wiring error in the station backplane effectively inverts the sense of the RST signal, so it is necessary to swap the RSTA / RSTB signals end to end in the cable as defined in the table below.* Additional comments related to CAN_GND and CAN_SHLD connections are included after the table.

DMC	← Cable is *NOT* straight through → Tensolite NF24Q100 Ethernet type 100BASE-T cable will be used. (two differential pairs)	**Station Backplane**

DB-9F Pin	**Signal**	**Description**	**DB-9F Pin**	Pair assignments
1	RSTA	RS-485 differential "bar" signal	***6***	Pair #2 Blu
2	CAN_L	CAN_L bus line (dominant low)	2	Pair #1 Red/Blk
3	CAN_GND	not connected		
4				
5	CAN_SHLD	Shield	***3***	Shield
6	RSTB	RS-485 differential "true" signal	***1***	Pair #2 Blu/Blk
7	CAN_H	CAN_H bus line (dominant high)	7	Pair #1 Red
8				
9				

Per [RD 09], section 2.1.2, CAN_SHLD at pin 5 on the DMC end connects to the outer shield of the cable and at each slave node it connects to the rack / module chassis. It further specifies that CAN_GND will be connected to the CAN transceiver at the bus master and that the use of CAN_GND within slaves is optional. Earlier versions added to this to say "the recommended use is to connect it to local ground through a small resistor (10-100 ohms)".

As designed, the Station Backplane has a small resistor connected between pin 5 and the backplane power ground layer. Pin 3 is connected directly to the backplane power ground layer. There is no separate connection to the rack chassis. The backplane ground layer is the only ground connection provided.

The CAN_GND pin at the DMC end (pin 3) has no connection in the cable. The CAN_SHLD pin at the DMC end (pin 5) connects to the cable shield and at the station backplane end, the shield connects to the station backplane ground layer via pin 3.

14 Correlator CAN Bus Configuration Options

In order to limit the total length of individual CAN buses and to limit the number of nodes per bus, Version A of this document specified that a total of nine individual correlator CAN buses were required. There were two buses per correlator quadrant that together served all SCC, LTA, Final Adder and DPI slave nodes. One additional bus served the four QCC cards, distributed across the four quadrants.

Preliminary tests in the first quadrant have demonstrated that it is likely we will be able to operate reliably with fewer buses. The preferred option requires a total of five buses, one per quadrant plus one for the four QCC cards. A second option requires a total of six buses, one per quadrant that excludes the DPI cards, plus one bus that serves all 16 DPIs, distributed across the four quadrants, plus the QCC bus.

Limiting the total number of buses required to six maximum is desirable since this is compatible with the current CCC implementation where only one CAN module (with six ports) is supported. It is also highly desirable that all SCC and LTA in a quadrant be on a single bus. This enables many internal tests to be implemented independent of CCC.

For these reasons, this version of this ICD specifies the preferred option with a total of five buses. This is with the understanding that if subsequent operations do not continue to demonstrate robust operation, then a later version will present the next option, where six buses are required, or if need be the original option where nine buses are required.

It should be noted that even with the original option where nine buses are required for the full four quadrant system, interim operation with two full quadrants would still only require five buses total and thus only one CAN module in CCC.

15 DRX CAN Bus Routing in Correlator

There are a total of 8 DMC CAN busses in the 4 quadrants of the correlator. The following sketch shows the general nature of the physical routing of the DRX CAN bus in one half of one quadrant. The cable from one of the DMC's follows the shortest path permitted by the cable trays to the "inner" of two station racks. . If necessary, it may be routed through a pair of correlator racks to reach the entry point to the DRX CAN bus in a pair of station racks. The bus then daisy chains through the pair of racks as shown in Figure 15.1 and is terminated at the far end.

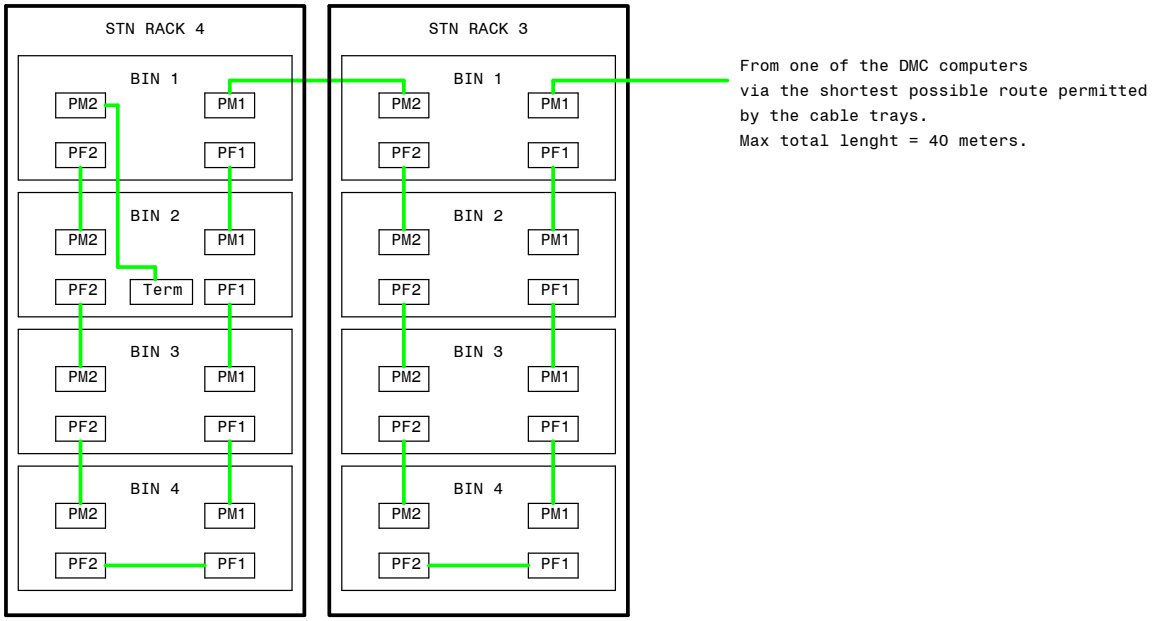


Figure 15.1 Sketch showing the routing of the DMC CAN bus (in green) in two statons racks. The cable should follow the shortest path to the DMC. Routing through cable trays in Correlator Racks is permissable.

The termination module provides the line to line 120 ohm CAN termination and a three resistor network to provide a "safe" termination for the RS-485 RESET line. If there is no driver for the RESET line, the RS-485 receiver will be presented with a non-asserted reset state.